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EXAMINER	
PETRANEK, JACOB ANDREW	
ART UNIT	**PAPER NUMBER**
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

mv

Office Action Summary	Application No.	Applicant(s)	
	10/531,610	REGNIER, LAURENT	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/14/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 are pending.

2. The office acknowledges the following papers:

Specification, claims, arguments, and terminal disclaimer filed on 9/25/2007.

Information Disclosure Statement

3. The previous citations 15-17 that weren't considered in the previous office action have been considered in this one.

Withdrawn objections and rejections

4. The specification objection has been withdrawn due to amendment.

5. The Double Patenting rejections for claims 1-3 and 6-8 have been withdrawn due to the filing of a terminal disclaimer.

6. The claim objections for claims 1, 4-5, and 7-8 have been withdrawn due to amendment.

Drawings

7. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations "so that the external analysis tool stores a time when the state of the output terminal is modified" from claims 1 and 7 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Each drawing sheet submitted after the filing date of an

application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d).

8. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. The objection to the drawings will not be held in abeyance.

New Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita (U.S. 6,467,083), in view of Trauben (U.S. 5,594,864).

11. As per claim 8:

Yamashita disclosed a method for monitoring a microprocessor executing a sequence of instructions by means of a device integrated to a microprocessor chip, the method comprising:

On each execution of an instruction from the sequence of instructions, generating a digital message corresponding to a type of the executed instruction (Yamashita: Figure 3 element 22, column 8 lines 9-26)(Information of the executed instruction codes and status of the instruction codes are passed from the data selector to the trace generator to generate trace packets.); and

Storing each generated digital message in a buffer memory (Yamashita: Figure 3 element 17, column 8 lines 27-38); and

An output terminal (Yamashita: Figure 3 element 24) connected to an external analysis tool (Yamashita: Figure 3 element 13).

Yamashita failed to teach modifying a state of one of a plurality of output terminals connected to an external analysis tool and each associated with an instruction type when a digital message corresponding to the instruction type to which said output terminal is associated is stored in the buffer memory.

However, Trauben disclosed modifying a state of one of a plurality of output terminals connected to an external analysis tool (Trauben: Figure 5 element 51, column 8 lines 26-30)(The output pins are changed on a cycle-by-cycle basis to provide information about the processor's execution.) and

Each associated with an instruction type when a digital message corresponding to the instruction type to which said output terminal is associated is stored in the buffer memory (Trauben: Figure 5 element 51, column 8 lines 48-67 continued to column 9 lines 1-7)(All of the terminals are associated with instruction types.).

The advantage of using a plurality of terminals in Trauben is that it allows the observation of important processor internal states in a cycle-by-cycle basis (Trauben: Column 8 lines 26-30). One of ordinary skill in the art would have been motivated by this advantage to implement the plurality of output terminals into the processor of Yamashita. Thus, one of ordinary skill in the art at the time of the invention to implement the output terminals of Trauben into the processor of Yamashita for the advantage of allowing observation of internal states in a cycle-by-cycle basis.

12. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita (U.S. 6,467,083), in view of Trauben (U.S. 5,594,864), further in view of Chen et al. (U.S. 5,642,478).

13. As per claim 9:

The additional limitation(s) of claim 9 basically recite the additional limitation(s) of claim 2. Therefore, claim 9 is rejected for the same reason(s) as claim 2.

14. Claims 1, 3, 5-7, 11-14, and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita (U.S. 6,467,083), in view of Trauben (U.S. 5,594,864), in view of Edwards et al. (U.S. 6,918,065).

15. As per claim 1:

Claim 1 essentially recites the same limitations of claim 8. Claim 1 additionally recites the following limitations:

Yamashita and Trauben failed to teach the external analysis tool stores a time when the state of the output terminal is modified.

However, Edwards disclosed the external analysis tool stores a time when the state of the output terminal is modified (Edwards: Figure 7 element 708, column 12 lines 29-35)(The combination with Yamashita results in trace messages with timestamps, that are passed via an output terminal to the external analysis tool.).

The advantage of using timestamps is that trace data generated by different functional units can be temporally correlated to properly debug a processing system. One of ordinary skill in the art would have been motivated by this advantage to implement trace timestamps onto the processor of Yamashita. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement timestamps in the processor of Yamashita for the advantage of being able to temporally correlate traces between different functional units.

16. As per claim 3:

Yamashita, Trauben, and Edwards disclosed the monitoring device of claim 1, wherein each output terminal (Trauben: Figure 5 element 51) is connected to a test terminal (Trauben: Figure 5 element 55, column 8 lines 23-26).

17. As per claim 5

Yamashita, Trauben, and Edwards disclosed the monitoring device of claim 1, wherein only certain types of instructions only are associated with an output terminal of the message calculation means (Trauben: Figure 5 element 51, column 8 lines 48-

50)(Only certain instructions will cause a message to be output via the output terminals.).

18. As per claim 6:

Yamashita, Trauben, and Edwards disclosed the monitoring device of claim 1, wherein each of the possible instruction types is associated with an output terminal of the message calculation means (Trauben: Figure 5 element 51, column 8 lines 48-50)(Only certain instructions will cause a message to be output via the output terminals. However, it's obvious to one of ordinary skill in the art that additional output terminals could be added so that all instruction types can be monitored for the advantage of being able to monitor all instructions executing in a program.).

19. As per claim 7

Claim 7 essentially recites the same limitations of claim 1. Claim 7 additionally recites the following limitations:

A microprocessor for executing a sequence of instructions (Yamashita: Figure 3 element 15, column 7 lines 26-39).

20. As per claim 11:

The additional limitation(s) of claim 11 basically recite the additional limitation(s) of claim 3. Therefore, claim 11 is rejected for the same reason(s) as claim 3.

21. As per claim 12:

Yamashita, Trauben, and Edwards disclosed the integrated circuit of claim 11, wherein a state of the test terminal is modified when a state of the output terminal connected to the test terminal is modified (Trauben: Figure 5 elements 51 and 55,

column 8 lines 23-26)(A change occurs at element 55 after a change occurs at element 51.).

22. As per claim 13:

Yamashita, Trauben, and Edwards disclosed the integrated circuit of claim 7, wherein, when at least two instructions of a first and a second type from the sequence instructions are executed in parallel (Trauben: Column 4 lines 32-41), the message calculation means generates a digital message corresponding to an instruction of a first type and modifies a state of an output terminal associated with the instruction of the first type and simultaneously generates a digital message corresponding to an instruction of a second type and modifies a state of an output terminal associated with the instruction of the second type (Trauben: Figure 5 element 51, column 4 lines 32-41 and column 8 lines 27-30)(The processor generates digital messages on the state of the processor on a cycle-by-cycle basis. The processor is also superscalar and is able to issue a plurality of instructions per cycle. Thus, it's obvious to one of ordinary skill in the art that since multiple types of instructions can be issued per cycle, multiple messages can be generated per cycle.).

23. As per claim 14:

Yamashita, Trauben, and Edwards disclosed the integrated circuit of claim 13, wherein the external analysis tool stores a time when the state of the output terminal associated with the instruction of the first type was modified and a time when the state of the output terminal associated with the instruction of the second type was modified (Edwards: Figure 7 element 708, column 12 lines 29-35)(The combination with

Yamashita results in trace messages with timestamps, that are passed via an output terminal to the external analysis tool. This results in traces for a plurality of different types of instructions having timestamps with their corresponding trace data.).

24. As per claim 16:

Yamashita, Trauben, and Edwards disclosed the integrated circuit of claim 7, wherein each output terminal from the plurality of output terminals is associated with a plurality of instruction types (Trauben: Figure 5 element 51, column 8 lines 48-50)(Only certain instructions will cause a message to be output via the output terminals. However, it's obvious to one of ordinary skill in the art that output terminals could be asserted for a plurality of instruction types for the advantage of being able to monitor all instructions executing in a program without having to add additional output terminals or to eliminate some output terminals. The advantage of eliminating output terminals is that costs are reduced.).

25. As per claim 17:

The additional limitation(s) of claim 17 basically recite the additional limitation(s) of claim 6. Therefore, claim 17 is rejected for the same reason(s) as claim 6.

26. Claims 2 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita (U.S. 6,467,083), in view of Trauben (U.S. 5,594,864), in view of Edwards et al. (U.S. 6,918,065), further in view of Chen et al. (U.S. 5,642,478).

27. As per claim 2, the rejection of claim 1 is incorporated and:

Yamashita, Trauben, and Edwards disclosed the monitoring device of claim 1.

Yamashita, Trauben, and Edwards failed to teach the buffer memory is divided into a plurality of areas, each of the areas is associated with a different instruction type and is intended to only store messages associated with said instruction type.

However, Chen disclosed the buffer memory (Chen: Figure 1 element 32) is divided into a plurality of areas (Chen: Figure 1 element 56), each of the areas is associated with a different instruction type and is intended to only store messages associated with said instruction type (Chen: Column 9 line 23-26)(Each divided buffer space stores traces for only a certain type or types of instructions.).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include different areas in the buffer memory and each associated to each instruction type in the system of Yamashita and Trauben because Chen teach that the inclusion would enable the correlation of trace data from different source(Chen Column 9 line 1-2). It enhances the capability of the accumulation of trace data information by organization of the information in the storage (Yamashita column 5 line 21-24).

28. As per claim 10:

The additional limitation(s) of claim 10 basically recite the additional limitation(s) of claim 2. Therefore, claim 10 is rejected for the same reason(s) as claim 2.

29. Claims 4 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita (U.S. 6,467,083), in view of Trauben (U.S. 5,594,864), in view of Edwards et al. (U.S. 6,918,065), further in view of Mihalik et al. (U.S. 4,574,354).

30. As per claim 4:

Yamashita, Trauben, and Edwards disclosed the monitoring device of claim 1.

Yamashita, Trauben, and Edwards failed to teach each output terminal is connected to an input terminal of a coding block comprising a predetermined number of coding block output terminals, each of the coding block output terminals is connected to a test terminal, each coding block being provided to have each of its n coding block output terminals switch once every n state switchings of its input terminal and so that a single one of its n coding block output terminals switches state at once.

However, Mihalik discloses each output terminal (Mihalik: Figure 1 element 12C) is connected to an input terminal of a coding block (Mihalik: Figure 1 element 16) comprising a predetermined number of coding block output terminals, each of the coding block output terminals is connected to a test terminal (Mihalik: Figure 1 element 14, column 7 lines 53-57)(Each bit of the output of a grey code counter is an output terminal of the coding block.), each coding block being provided to have each of its n coding block output terminals switch once every n state switchings of its input terminal (pulse emitted by TTA) and so that a single one of its n coding block output terminals switches state at once [the use Grey code (column 7 line 53-57)].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include encode state change in the output terminal by Gray code to be a encoded number in the system of Yamashita and Trauben because it is encoded the number of the time the state of input terminal change into a count (Mihalik column 7 line 53-57). It enhances the capability of the accumulation of trace data

information by collecting more information (the count of certain type of instruction executed in the processor) (Yamashita column 5 line 21-24).

31. As per claim 15:

The additional limitation(s) of claim 15 basically recite the additional limitation(s) of claim 4. Therefore, claim 15 is rejected for the same reason(s) as claim 4.

Response to Arguments

32. The arguments presented by Applicant in the response, received on 9/25/2007 are partially considered persuasive.

33. Applicant argues "Trauben failed to teach a plurality of output terminals connected to an external analysis tool, each output terminal being associated with one of the instruction types and the message calculation means modifying a state of the output terminal associated with an instruction type when a message corresponding to said instruction type is stored in the buffer memory so that the external analysis tool stores a time when the state of the output terminal is modified" for claims 1 and 7.

This argument is found to be persuasive for the following reason. The examiner agrees that Trauben failed to teach all of the limitations of this claim, including the newly added limitation where the external analysis tool stores a time when the state of the output terminal is modified. However, due to the amendment, a new ground of rejection has been given.

34. Applicant argues "Trauben failed to teach modifying a state of one of a plurality of output terminals connected to an external analysis tool and each associated with an

instruction type when a digital message corresponding to the instruction type to which said output terminal is associated is stored in the buffer memory" for claim 8.

This argument is not found to be persuasive for the following reason. Trauben disclosed in figure 5 element 51 that a state of the output terminals are modified on a cycle-by-cycle bases depending on the execution of the processor. Trauben also disclosed in columns 8-9 that the output terminals are associated with an instruction type.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Baird et al. (U.S. 5,848,264), taught using timestamps with tracing data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner, Art Unit 2183